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Abstract
Power amplifier is the key component for transmitter of system. It not only provides necessary power for wireless communication but also relate with linearity and efficiency.

Because of wireless communication develop quickly and many research reports have published. Power amplifier is not only focused in electronic property. In order to conform system request, many people use extra system or DSP(digital signal process) to improve linearity and efficiency. Good linearity and efficiency affect signal quality and power consumption, respectively. But in real life, linearity and efficiency can not coexist simultaneously. Therefore, how to choose the trade off between linearity and efficiency is the most important topic in the present day.

A two-stage power amplifier with on chip linearizer is designed in this thesis. Its property is listed as follows: Output power is 22.38 dBm, power gain is 21.8 dB, and power added efficiency is 32.2 %.
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